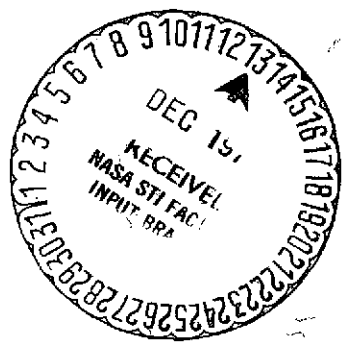
NASA SP-5972 (01)

TECHNOLOGY UTILIZATION

ELECTRONIC EQUIPMENT, SYSTEMS, AND TECHNIQUES

A COMPILATION



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Foreword

The National Aeronautics and Space Administration has established a Technology Utilization Program for the dissemination of information on technological developments which have potential utility outside the aerospace community. By encouraging multiple application of the results of its research and development, NASA earns for the public an increased return on the investment in aerospace research and development programs.

This publication is part of a series intended to provide such technical information. The items presented are divided into two sections. Section one consists of a selection of electronic circuits with specialized computer applications. The second section is comprised of electronic circuits that perform a variety of control functions.

Additional technical information on individual devices and techniques can be requested by circling the appropriate number on the Reader Service Card included in this Compilation.

The latest patent information available at the final preparation of this Compilation is presented on the page following the last article in the text. For those innovations on which NASA has decided not to apply for a patent, a Patent Statement is not included. Potential users of items described herein should consult the cognizant organization for updated patent information at that time.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this Compilation.

Jeffrey T. Hamilton, *Director*
Technology Utilization Office
National Aeronautics and Space Administration

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Contents

Section 1. Specialized Computer Circuits

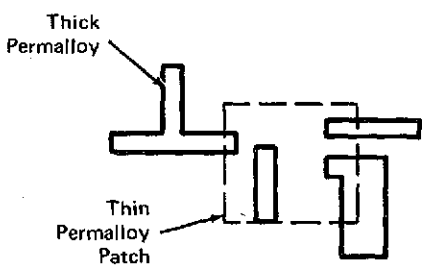
PERMALLOY PATCHWORK IMPROVES BUBBLE-DOMAIN MEMORY DEVICE

The operation of bubble-domain memory devices is improved by the application of small patches of thin permalloy over selected components. This lowers the effect of the bias field, improves the operating margin of the overall device, and increases its reliability.

Structurally-integrated bubble-domain memory devices are fabricated by evaporation and electroplating. Conventional photolithography produces masks for exposing the photoresist used to form the necessary structures. Then the thin permalloy film is etched away to outline the magnetoresistive sensor and the open areas between conducting lines, so that no short-circuit conditions exist.

Protecting certain areas with photoresist, to permit the thin film to remain, reduces the effect of the bias field locally in these areas and allows the bubble to expand slightly. If a bubble collapses or is forced out of a thick permalloy structure, a small patch of permalloy causes the bubble to expand and thereby remain on the structure.

Laboratory tests indicate that the bias field at which a bubble elongates into a serpentine pattern and the field at which it dissipates are both reduced by approximately five amperes/meter in the presence of a thin (200-Angstrom) permalloy patch. Thus, the operating range of this memory device can be adjusted by selectively placing thin permalloy patches over the thick permalloy segments, as shown in the figure.



Thin Permalloy-Patched Bubble-Domain Component

Source: R. J. Hendel, T. F. Jamba, Jr., G. E. Keefe, and L. L. Rosier of IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-22116)

Circle 1 on Reader Service Card.

COMPACT DECODER FOR BUBBLE-DOMAIN MEMORIES

Early bubble-domain memories, like semiconductor memories, used 2n decode lines to select one of 2^n shift registers. Thus, much of an integrated circuit chip had to be used for shift register selection.

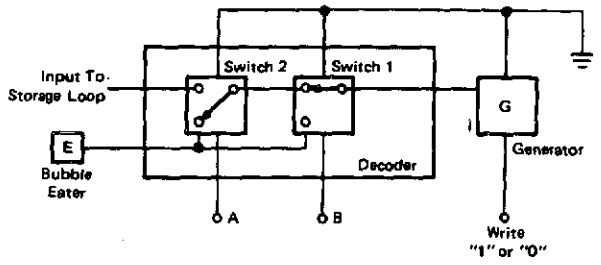


Figure 1. Conventional Write Section of Bubble-Domain Decoder

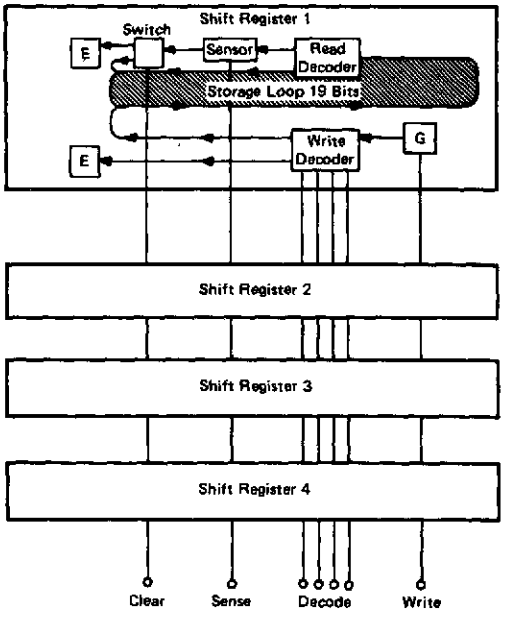


Figure 2. Current-Controlled Bubble Generator

Single-pole double-throw switches provide a more compact decoder for a bubble-domain memory. By placing complementary switches at the control-line crossing with each shift register, less chip area is required to decode the memory. This arrangement reduces the space and the delay time required to one-half.

A write section of a bubble-domain decoder consists of two parallel bubble paths with a number of "bridges," where a bubble may cross from the upper path to the lower path. Each bridge has a current-carrying control line, which determines whether a bubble will cross over a bridge. The memory is designed so that each shift register has a corresponding current-controlled bubble generator. The control lines of all the generators are wired in series to produce a single write line. Depending on the binary input to this write line, one of two things happens during each field rotation: either each generator emits a bubble, or none do. A "one" is written into the single register chosen from the 2^n shift registers, by having all 2^n generators emit a bubble. Then 2^n-1 bubbles are steered into bubble annihilators (eaters).

The decoder section (Figure 1) is used to write the "ones". The generator is connected to the upper-path input, and the bubble eater is connected to the lower-path output. The upper-path output leads to the storage loop of the shift register. The bubble starts traveling from the generator along the upper path but must pass every bridge without being shunted to the lower path, in order to remerge into the storage loop. This happens in only one of the 2^n shift registers. The read decoder fuctions in line manner, as shown in Figure 2.

Source: G. S. Almasi and G. E. Keefe of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-21914)

Circle 2 on Reader Service Card.

BIAS-FIELD EQUALIZER FOR BUBBLE-DOMAIN MEMORIES

The transverse magnetic bias field required to maintain cylindrical magnetic domains or "bubbles" in a domain memory must be held constant to within ± 16 percent.

If a magnetic platelet is exposed to a perpendicular magnetic bias field of appropriate amplitude, cylindrical domains are formed in the platelet and are perpendicular to the bias field. With a too high perpendicular field, bubbles will collapse; with a too low field, bubbles will elongate to serpentine domains. For a magnetic platelet by itself, the allowable variation from the median bias field is typically ± 16 percent, with the maximum-to-minimum diameter ratio equal to 3. In practice, however, the tolerance is lower.

Permanent magnets are the preferred source for the perpendicular bias field because they weigh less than equivalent bias-field coils. They require no operating power and are relatively nonvolatile. However, over long periods of time, the magnetization of the permanent magnet may change enough to affect adversely the operating margins of the memory, by either collapsing or overly expanding the bubbles.

The ± 16-percent tolerance can be maintained with a magnetoresistive permalloy sensor monitoring the bias field. The sensor generates error signal used to correct the magnitude of the bias field. For maximum sensitivity, the sensor magnetization is oriented at an angle of 45° to the measuring current for the nominal value of the bias field. For a 100-oersted bias field and a sensor thickness of 1000 Angstroms, the sensor width should be 5 micrometers.

The error signal from the sensor can be used to control the magnitude of the bias field in one of the following ways: (a) An auxiliary set of bias-field coils may be provided around the permanent magnet field; (b) The sensor output may be used to control the magnetizing current through the auxiliary coils, to aid the existing permanent magnet field; or (c) The current in the small coils may be used to remagnetize the permanent magnet. This remagnetization can be done by a very infrequent, short, high-current pulse or by a short sequence of pulses. The magnetizing current pulses would consume very little power over the life of the memory.

Source: G. S. Almasi and G. E. Keefe of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-21913)

Circle 3 on Reader Service Card.

THERMAL CONTROL OF OPERATING MARGINS IN BUBBLE-DOMAIN MEMORY DEVICES

There are instances when bubble-domain memory devices may have functional components with magnetic operating margins that are incompatible with other functional components. In such cases, the entire magnetic device becomes inoperable.

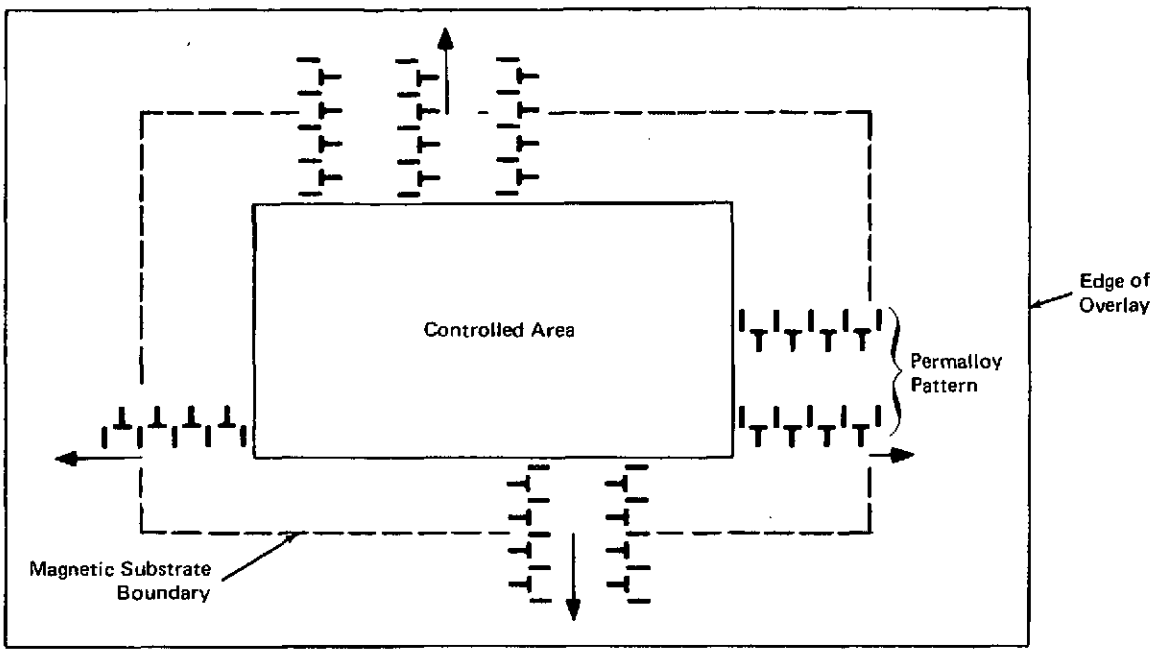
The magnetic operating margins of the incompatible components may be altered by raising the temperature of the portion of the device containing them, in order to achieve total device operation. The operating margins of the bubble-domain memory devices are temperature sensitive, to the extent that bubble diameter and saturation magnetization vary with temperature.

In some bubble materials, this dependence is significant; it can be used to remedy the situation in which all components of a bubble-domain device have overlapping operating characteristics, with the exception of one set of components, e.g., generators, splitters, or annihilators. Temperature can be increased in areas of the device (for example, by resistive heating through a strip line), and margins can be made compatible with other components. In the special case of the saturation magnetization decreasing as temperature increases, annihilation can be accomplished by leading the bubble into the local hot spot.

Source: G. S. Almasi and L. L. Rosier of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-22115)

Circle 4 on Reader Service Card.

EDGE EFFECT IMPROVES BUBBLE-DOMAIN MEMORY DEVICES



Modification to Bubble-Domain Memory

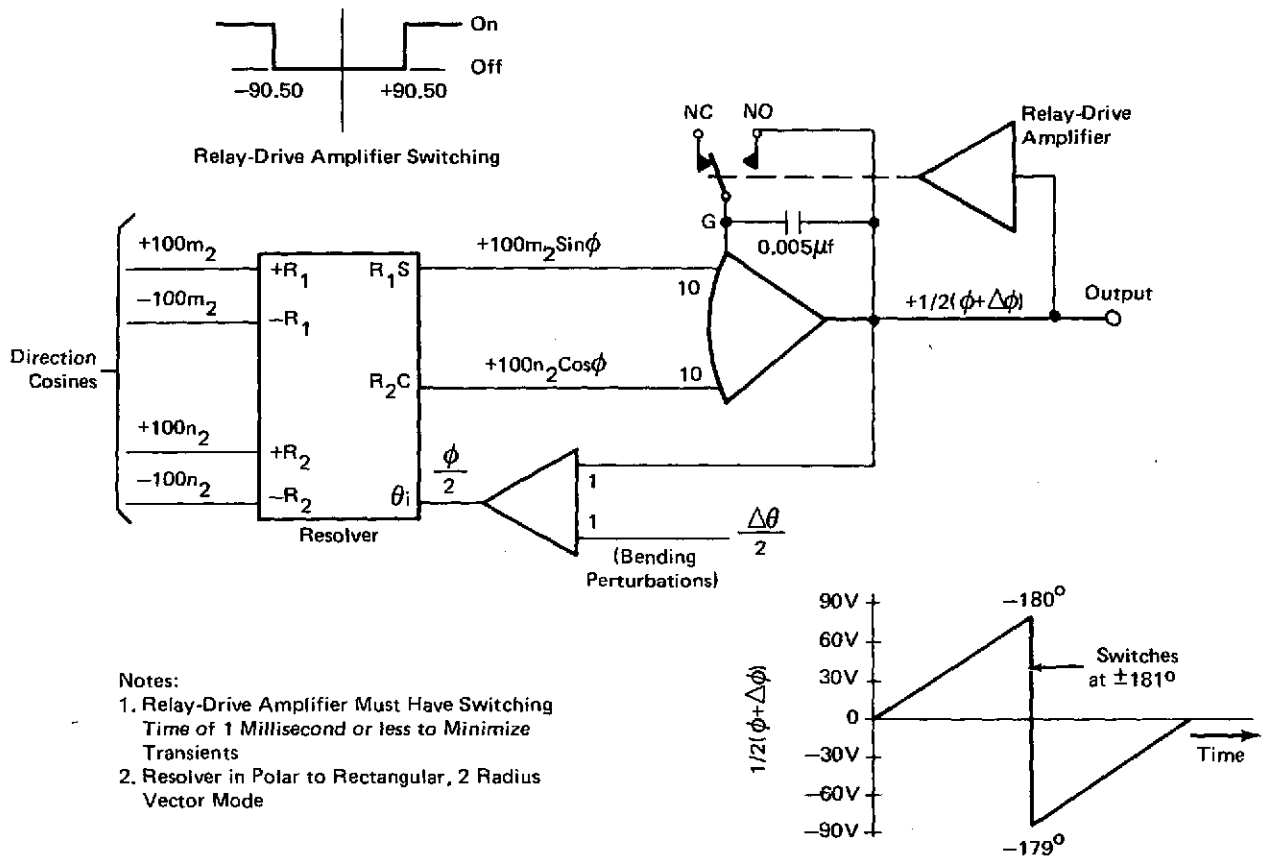
Bubble-domain memory devices may lose magnetic bubbles from the controlled areas. This will lead to memory errors if the bubbles accidentally reenter the controlled area. Straying bubbles can be intercepted and guided to the edges of the device where they will lose their magnetic charge and collapse.

An arrangement of permalloy patterns is used to provide bubble-directing paths from all sides of the controlled area to points beyond the magnetic substrate boundary (see figure). Any free bubbles are thus guided to points where they collapse and are unable to return to the controlled area.

Source: G. S. Almasi, G. F. Keefe, and L. L. Rosier of IBM Corp. under contract to Marshall Space Flight Center (MFS-22114)

Circle 5 on Reader Service Card.

MODIFICATION OF IMPLICIT ARC TANGENT GENERATION FOR CONTINUOUS ROTATION



Continuous Rotation Arc-Tangent Generator

A conventional analog-computer electronic-inverse resolver can be modified to permit increase of the computed arc-tangent angle for continuous rotation. The modification consists of very briefly dropping the resolver output angle to zero whenever its magnitude reaches 181° (see figure). This causes the circuit to switch to the opposite-polarity equivalent angle which has a magnitude of 179°.

The use of implicit arc-tangent generation-of-attitude angles for a continuously rotating body has been successfully employed to provide attitude angles for Skylab analog simulation.

Source: R. D. Hilborn of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-17315)

No further documentation is available.

SPECIAL-PURPOSE CONICAL-SCAN/STRAIGHTENER DEVICE: A CONCEPT

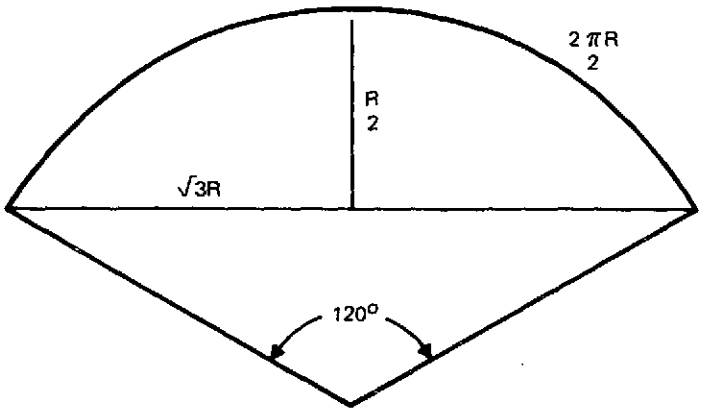


Figure 1. Geometric Relationship Between Conical and Straight Scans

Conversion of the output of conical-scan sensors into straight-line scans of equivalent resolution, using present general-purpose computer techniques, is time consuming and requires an excessive amount of money. Relatively-inexpensive, special-purpose computer hardware has been conceived that could convert a conical scan to a straight-line scan.

For equivalent spatial resolution, the conversion of conical scans to straight-line scans reduces the number of data points by approximately 17 percent. Thus, for every 100 evenly spaced points along the conical scan, there will be 83 evenly spaced points along the straight-line (straightened) scan. In a typical conical-scan sensor, only information from the forward 120° (Figure 1) of the scan is used. Conical scans of length, $2\pi R/3$, are straightened (converted) to straight scans of length, $\sqrt{3}R$, in this case.

A straightened scan is shown mapped across several conical scans in Figure 2. The geometry (as illustrated in Figure 1) will show that a single straightened scan of N data points will map across approximately 0.288N conical scans, each of which contains 1.2N data points. If the straightened scans are derived from the conical-scan data by nearest-neighbor assignment (i.e., if the straightened scan is mapped across the conical-scan data, and the value assigned to each point on the straightened scan is the value of the nearest conical-scan point), the value of the conical-scan data point assigned to any given straightened-scan data point is dependent upon the geometry of the problem and can be determined mathematically. Furthermore, the location of each straightened-scan data point, relative to the surrounding conical-scan points, is invariant.

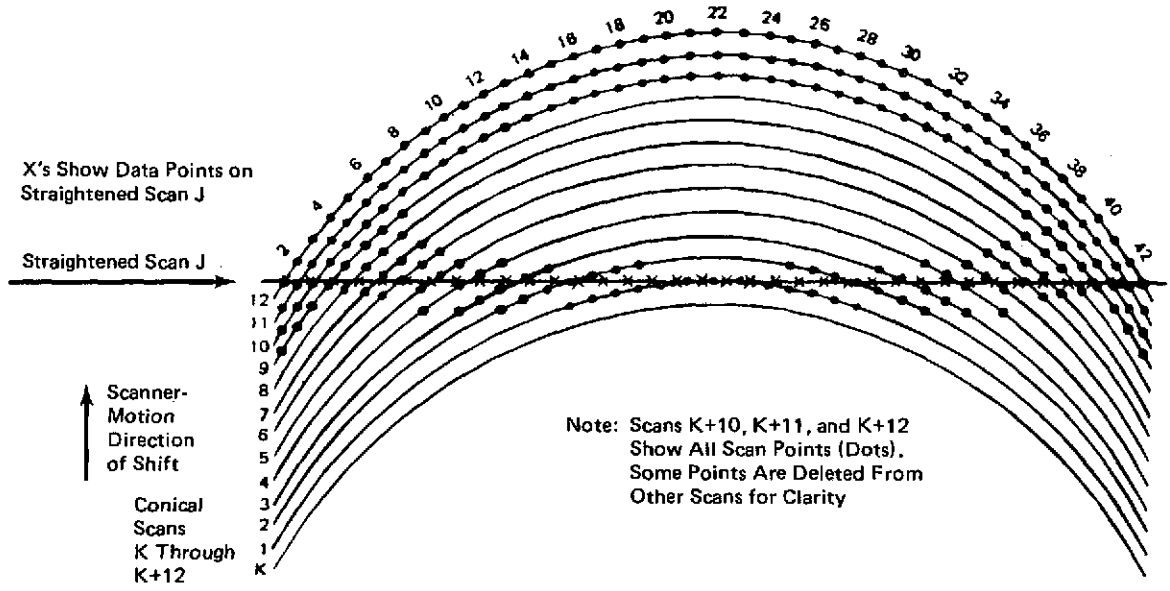


Figure 2. Straightened Scan Mapped Across Conical Scans

These points are shown in Figure 2 by thirteen consecutive conical scans, labeled K through K+12, and one straightened scan labeled J. The figure also shows where the 37 points of the straightened scan lie in relation to the 43 points of each conical scan. Nearest-neighbor assignment will select point 1 of conical scan K+12 for point 1 of the straightened scan J, point 3 of scan K+10 for point 2 of scan J, point 4 of scan K+9 for point 3 of scan J, etc. The first three points of straightened scan J-1 will represent point 1 of scan K+11, point 3 of scan K+9, and point 4 of scan K+8. The first three points of scan J+1 will represent point 1 of scan K+13, point 3 of scan K+11, and point 4 of scan K+10. Thus, it is seen that as the straightened scan index changes, the conical-scan index will change correspondingly in a fixed manner.

Source: D. G. Ferneyhough, Jr., and
C. T. Landers of
IBM Corp.
under contract to
Marshall Space Flight Center
(MFS-22718)

Circle 6 on Reader Service Card.

ABEL-INVERSION COMPUTATION

1. Leads marked "s" must be short.
2. 1M resistors are 0.1 percent.
3. Potentiometers are 1K, 10 turn, 0.1 percent Lin unless otherwise noted.
4. Bias batteries are 1.34V mercury cells.
5. Ground circuit at one point only.
6. All switches are ganged to a single shaft. The switch is labeled "emitter density" and its 10 positions correspond to J = 0, 1, ... , 9.

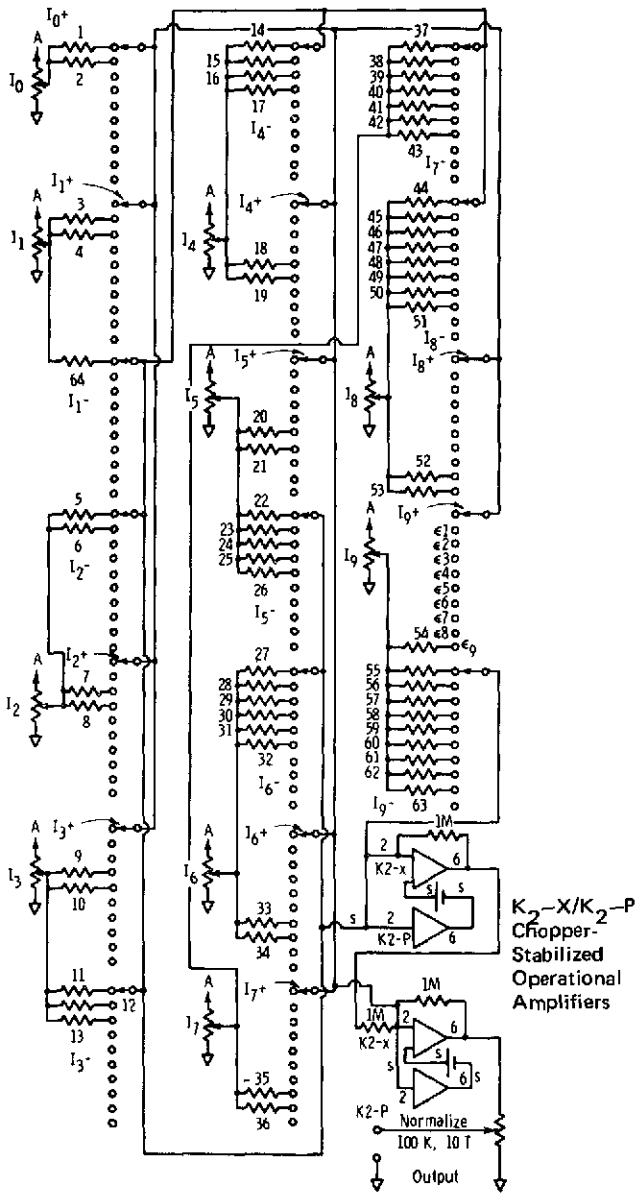


Figure 1. Simplified Schematic of Abel-Inversion Computer

To calculate the radial distribution of emitters within a cylindrical plasma from the observed radiation, an electronic analog uses a numerical integration to perform Abel inversion. The emitter density at a given radial position r is

$$\epsilon_j = \sum_{k=j-1}^{9} A_{jk} I_k(x)$$

where ϵ_j is the emitter density, $I_k(x)$ is the observed intensity at the position x_k, and the A_{jk}'s are coefficients given by Bockasten, "Journal of the American Optical Society," Volume 51, page 943, 1961.

The electronic analog uses a switch-selected resistance network to form the A_{jk} coefficients and uses two chopper-stabilized operational amplifiers to perform the addition and subtraction in the above series. Ten values of the intensities are represented by potentiometer settings, and the emitter density is read by means of a digital voltmeter (see figure).

An understanding of how the computer operates may be obtained by noting the circuitry involved in computing the emitter density ϵ_7, where

$$\epsilon_7 = 0.171\ I_6 + 1.465\ I_7 - 1.071\ I_8 - 0.087\ I_9$$

To perform this calculation, all of the rotary switches shown in the figure are placed in the ϵ_7 position, which is the eighth contact from the top of each switch. The intensity potentiometers I_0 through I_5 are inoperative, since there is now no path between them and any of the switch rotors. A path exists for the I_6 and I_7 potentiometers to the plus amplifier by way of R-34 and R-35, respectively. Similarly, connections are made from the I_8 and I_9 potentiometers by way of R-51 and R-62 to the minus amplifier; and this output, which is $-1.071\ I_8 - 0.087\ I_9$, is entered into the input of the plus amplifier. Resistances R-34, R-35, and the 1-megohm resistor at the input of the plus amplifier have been chosen so that its output consists of $-\epsilon_7$. Although the output of the computer is the negative of the desired emitter density, this should not prove any hindrance since only the magnitude is used.

The values of the resistances required in the summing network are given in the table. Tests of the accuracy of the computer described have been run with both experimental and analytic intensity distributions. The inversion was found to agree with a more exact method to ±1.5% but sometimes failed near the center due to the use of only 10 data points.

Source: Roman Krawec
Lewis Research Center
(LEW-10879)

No further documentation is available.

REPEATED SINGLE-ERROR CORRECTION CAPABILITY

Reliability in computer memory modules has been improved by redundancy. Unfortunately, this is expensive in terms of module weight and volume. Error-correction codes, on the other hand, require only a fraction of such added weight and volume in a complete module.

Sense-line component failures cause single-bit errors, are random, and require the ability to correct a single bit at a time.

The memory module features a repeatable single-error connection capability plus a serial-data-shift register. It also has a second shift register, loaded by external control, and an external map of existing faulty-sense lines within the module. A faulty-sense line represents a significant class of failure which affects one bit within a limited-address range. The external map stores beginning and ending addresses of this range and a faulty-bit identifier. When access is required between these addresses, the faulty-bit location is loaded into the second shift register.

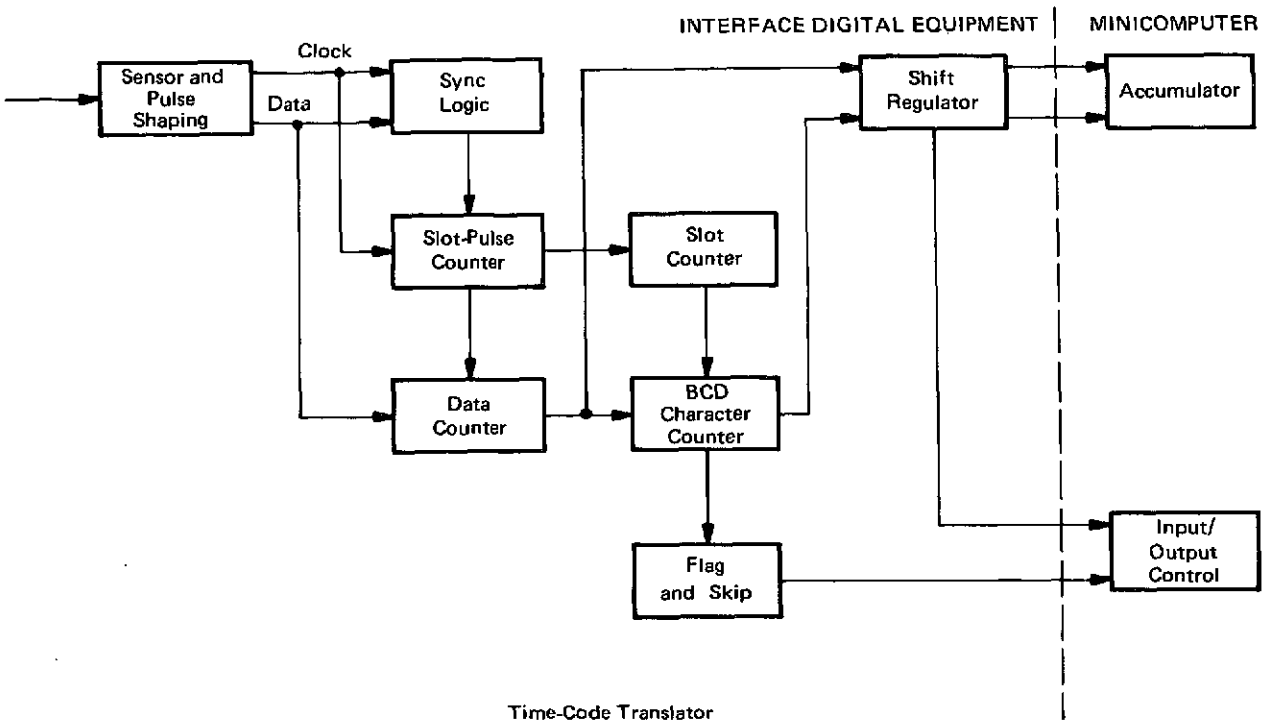
The operational description assumes a read mode; the write mode requires a reversal of the sequence of events. In the read mode, data transfer is from the storage media to the data-shift register. Control circuitry sets the faulty-bit position to a zero. The registers advance normally until the faulty-bit indicator in the second register triggers a modification. An extra pulse to advance the data-shift register then advances all remaining bits one position, without a transmitted bit. The faulty bit is now completely masked, and the gap left is filled by the next bit. A bits-per-word-transmitted counter, required for transmission control, will not count a complete word until the required number of bits have been transmitted. The final transmitted bit is the spare bit.

This sequence thus removes the faulty bit from a word being checked for correctness. Once removed, the check circuitry is available to correct another single-bit failure. This correction capability can be reinstated as many times as there are spare bits available.

Source: A. L. Recksiedler of
Sperry Rand Corp.
under contract to
Marshall Space Flight Center
(MFS-22332)

Circle 7 on Reader Service Card.

TIME-CODE TRANSLATOR



Time-Code Translator

A time-code translator can be used with data-retrieval media such as magnetic tapes or disks on which the time code has been recorded serially. It can receive process commands remote from a central processor by telephone line or other hard-wire communications. The translator provides a means of interfacing the NASA 36-bit time code from a time-code generator to a using device such as a computer. The translator strips out the serial binary-coded decimal (BCD) information from an amplitude-modulated 1000-Hz carrier. Thus, wherever a real-time reference is needed, the device will store parallel data into a register for direct input to the using equipment.

The level-sensing technique at the translator input permits the system to be used with a large variety of input devices such as magnetic tape. The level sensor has a differential amplifier input, thus isolating the carrier-level shift normally associated with magnetic-tape input. It also includes built-in high-frequency noise rejection.

Sync logic (see figure) is used to start the slot-pulse and data counters at the beginning of a data slot (DS) detected by the sensor. The clock pulse that occurs with data present sets the sync and is counted as the first count in the slot-pulse counter. This counter is wired as a modulus 10 counter; the 10th count is decoded as a DS pulse. The third state of the slot-pulse counter is sampled at a DS time to determine whether the data is a logic "1" or "0". In the reset stage, every DS pulse transfers the data count into the first stage of the shift register.

Each decoded count of 3 adds 1 into the BCD character counter, a modulus 9 counter which resets at count 9. At that time, if the enable time code has been set by the computer program, the shift-register pulses are inhibited and the time-code flag is set. No further time codes are processed until the computer resets the flag. The time code is in the shift register and is read-in on two computer program words. When the flag is reset, the translator system will begin a search for the next reference marker.

Source: David F. Parker of
Martin Marietta Corp.
under contract to
Goddard Space Flight Center
(GSC-11218)

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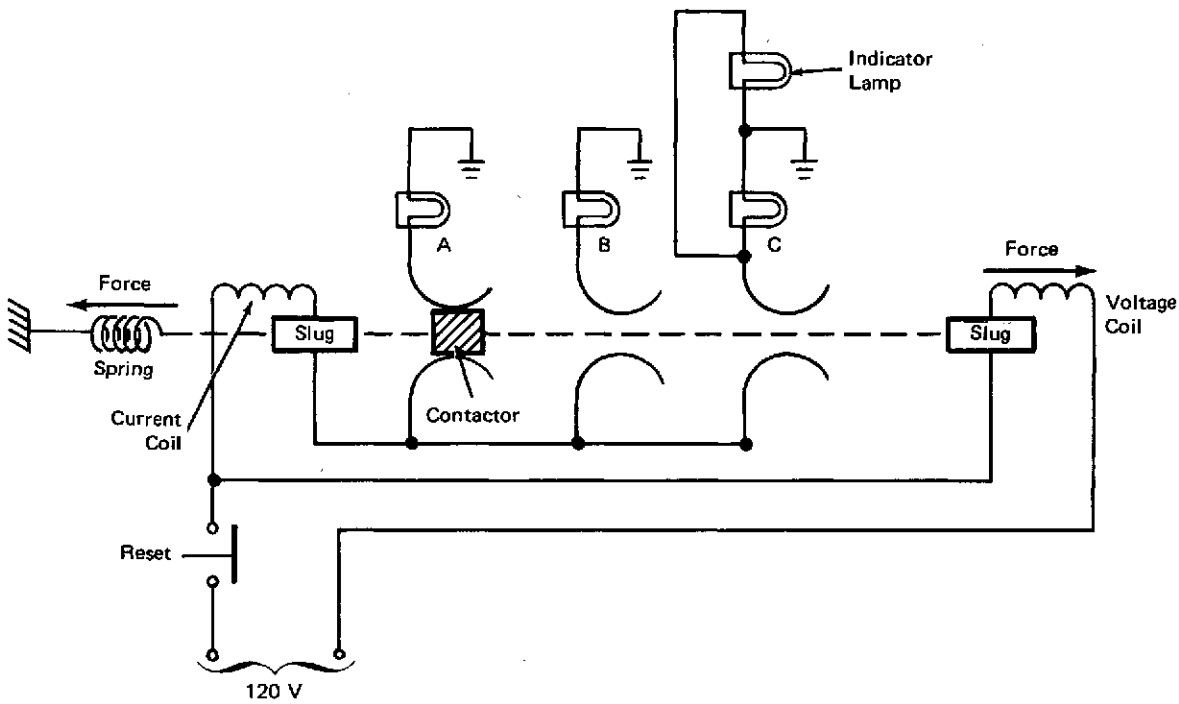
Section 2. Control Circuits

AUTOMATIC LAMP CHANGER



Three-Lamp System

In some applications, replacement of incandescent lamps is particularly difficult. In addition, lamps such as emergency-exit lights should not be allowed to go out, even for the limited period of time required to detect burnouts. For applications such as these, an automatic lamp changer has been developed. Three lamps can all be installed at one time; each lamp will burn its full life and then turn the next lamp on automatically.

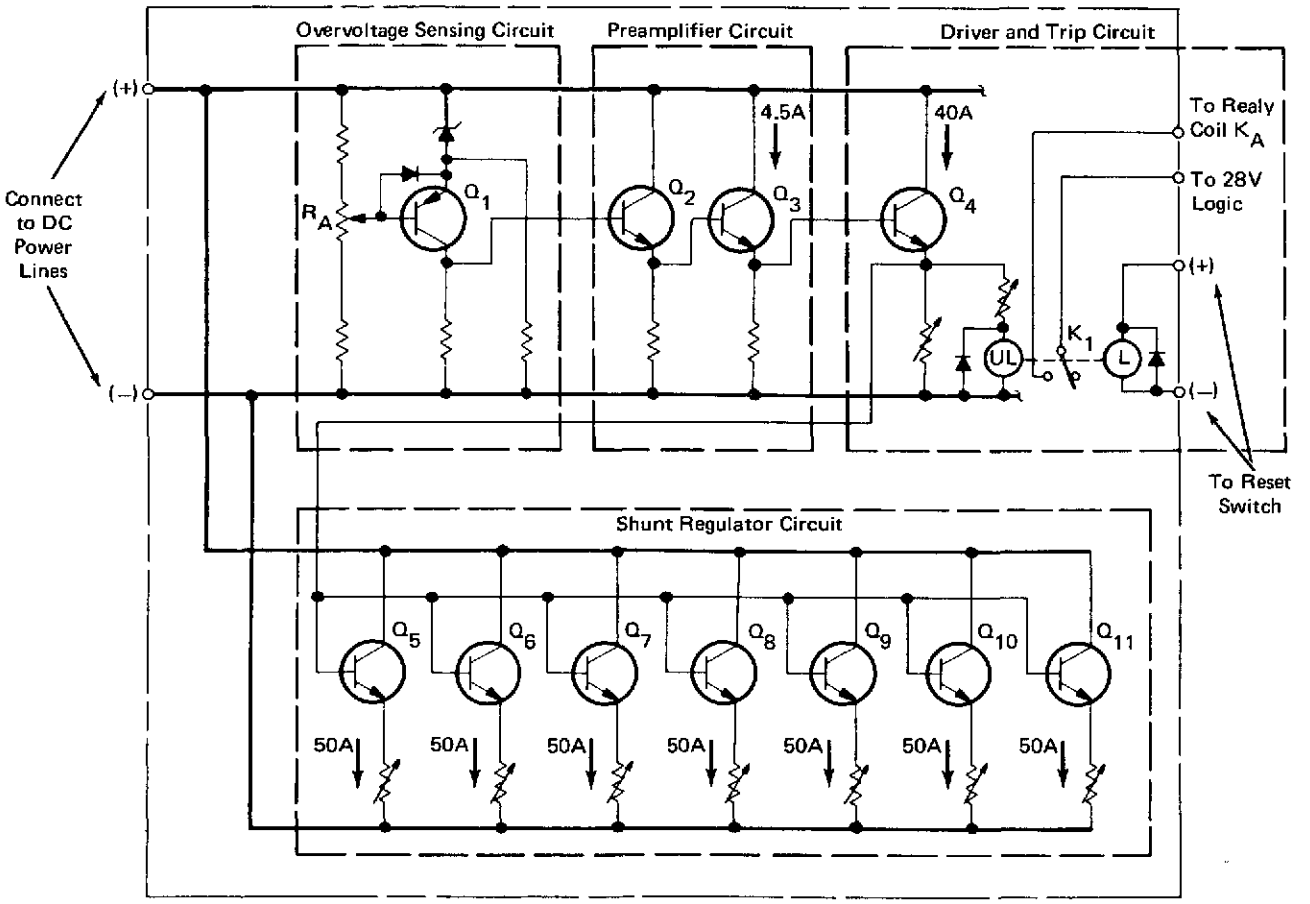
The operation of the system is shown in the figure. The spring pulls the contactor to lamp A. While lamp A is operative, the forces from the voltage and current coils balance the contactor in position for lamp A. When the lamp burns out, the voltage coil pulls the contactor to lamp B where the forces then balance.

When the last light (lamp C) is burning, the indicator lamp lights up; the first two lamps can then be replaced. The reset button is used to return the contactor to lamp A after all three lamps have burned out.

Source: R. R. Peck of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-15745)

No further documentation is available.

HIGH-CURRENT OVERVOLTAGE DETECTOR AND VOLTAGE-LIMITER CIRCUIT



Figire 1. 400-A Overvoltage-Detector Voltage-Limiter Circuit

Very high current power supplies (100 amperes or more) incorporate overvoltage protection within the supply itself. Response time for shutdown in an overvoltage situation is usually 50 ms approximately. This can result in interruption by transient power surges well within the capacity of the load. The overvoltage-detector voltage-limiter circuit, on the other hand, permits reasonable transient overloads of up to 500 ms duration without power interruption, thus maintaining critical loads "online" within their design capacities.

The 400 amperes dc overvoltage-detector voltage-limiter circuit consists of four states (Figure 1): (1) an overvoltage sensing circuit, (2) a preamplifier, (3) a driver trip circuit, and (4) a shunt regulator circuit. In operation, transistors Q_1 and Q_{11} are "off" until an overvoltage condition exists. Trim potentiometer R_A is set to make Q_1 conduct at 39 V dc (system overvoltage threshold). As this occurs, Q_1 causes Q_2 through Q_{11} to conduct, thus holding the line voltage at 39 V dc. This overvoltage condition must continue for more than

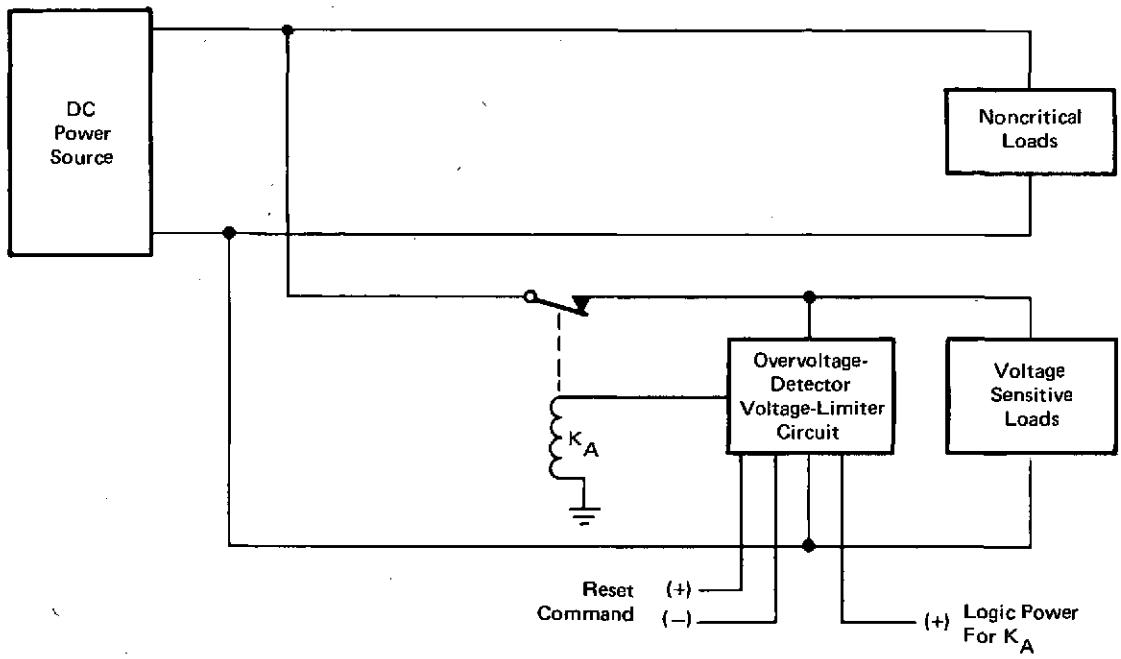


Figure 2. Typical Application Circuit

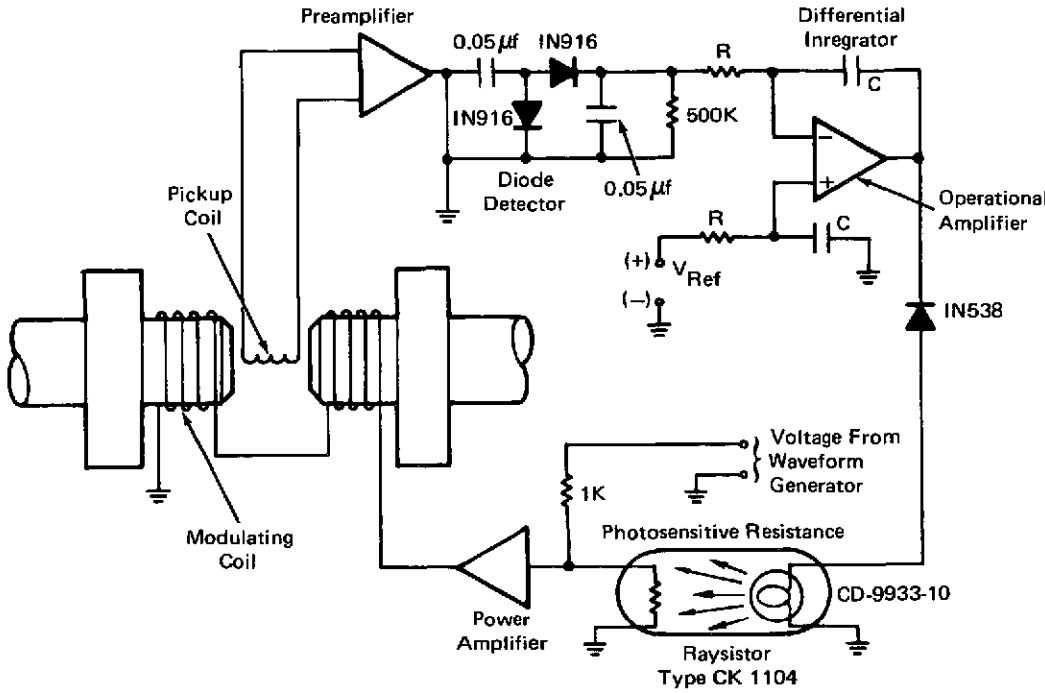
500 ms before time-delay relay K_1 is tripped, to disconnect the load from the power supply. K_1 must be reset after each shutdown.

Figure 2 shows the overvoltage-detector voltage-limiter circuit in a typical application. It illustrates the ability to place the circuit close to the load or in any position most convenient considering possible voltage-line losses.

Source: W. J. Wong of
Rockwell International Corp.
under contract to
Johnson Space Center
(MSC-19219)

No further documentation is available.

AUTOMATIC DISTORTIONLESS CONTROL OF MAGNETIC FIELD MODULATION



Closed-Loop Mode Control Circuit

Closely controlled magnetic field modulation is required when using such fields in magnetic-moment or resonance experiments or in determining the magnetic properties of materials. Close control is often difficult due to nonlinearities in the magnet or in the surrounding material. For example, a given level of modulation current in a magnet, particularly in an iron core magnet, does not generate the same level of field modulation over widely varied dc fields. This is especially true as magnetization of the core nears saturation.

The problem is eliminated by the closed circuit shown in the figure. The system uses a light-sensitive resistor as one leg of an attenuator, which adjusts the modulation-amplifier drive signal. Appropriate control of the illumination incident upon the photocell compensates for changes in core magnetization with change in the field.

The correction signal is derived as follows. The modulation component of the field is sensed by a pickup coil, preamplified, and converted by the diode detector to a dc voltage. This generates a voltage proportional to the actual field modulation amplitude present. Comparison of this voltage against a dc reference voltage in a differential integrator produces an output to control the illumination of the photocell.

When the input voltages to the integrator are equal, its output remains steady. Any error between the two inputs causes the output to vary, readjusting the attenuation of the modulating signal. With the proper phasing, the attenuation can be controlled to restore the field modulation to its desired level, reducing the error to zero. Thus, the desired level of modulation is set by the reference voltage.

Closed-loop instabilities can be avoided by limiting the speed of response of the system. This is easily accomplished through proper selection of the integrator RC time constant.

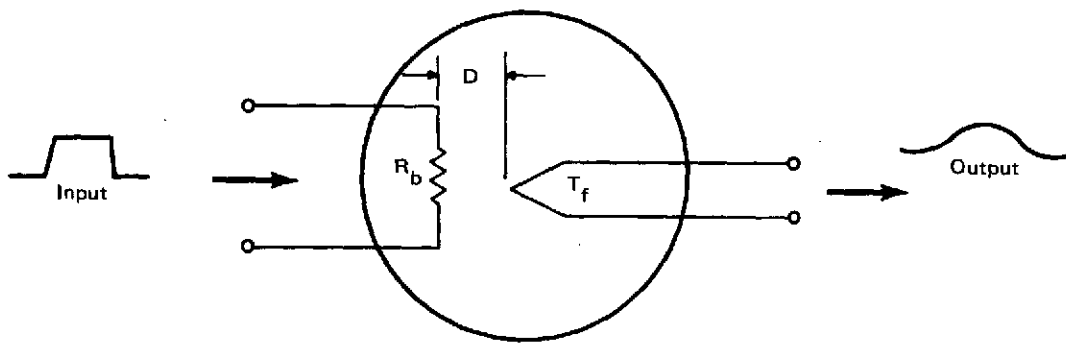
A diode was included in the lamp circuit to render the lamp inoperative, should the integrator output be driven through zero. Without it, the signal phasing would become inverted effectively in such a situation, and the system would be driven away from equilibrium.

Essentially, this control system has four advantages. First, the passive nature of the photovariable resistive attenuator introduces no distortion. Second, the photocoupling can be used to provide isolation, should ground loops present a problem. Third, unlike many control schemes which can reduce only proportionally an error between the actual modulation level and its desired level, this scheme reduces that error to zero. Fourth, since the modulation level is voltage controlled, a time-varying reference voltage may be used to vary the modulation amplitude relative to time.

Source: Russell J. Jirberg
Lewis Research Center
(LEW-10953)

No further documentation is available.

THERMOELECTRIC LOW-FREQUENCY DC ISOLATOR: A CONCEPT



Thermoelectric Low-Frequency DC Isolator

A new method has been proposed for transferring information between two dc isolated circuits. The principle (see figure) involves the use of a bismuth/antimony thin-film thermocouple in combination with a bridgewire resistance device in close proximity. The bridgewire resistance value (R_b) may be varied to fit specific drive-circuit power constraints. Power input must be sufficient to heat the bridgewire to greater than 450 K (350° F) but less than the white-hot temperature of the bridgewire material. The ac signal is superimposed on the bridgewire creating current analogous to modulation on a carrier. The output voltage of the thin-film bismuth/antimony thermocouple (T_f) can be varied from 1 mV to 10 mV by adjusting the distance (D) between the thermocouple and the bridgewire.

Source: Aubrey J. Butts of
Martin Marietta Corp.
under contract to
Langley Research Center
(LAR-11102)

No further documentation is available.

WATT-HOUR AND AMPERE-HOUR METERS

Two similar electronic meters have been designed; one measures watt-hours, and the other measures ampere-hours. They will determine, respectively, the watt-hours or ampere-hours put into a battery during charge as well as the hours removed during discharge.

The meters are used primarily to measure dc. Both are simple, very accurate, provide an analog output and have a meter display. Their dynamic range is wide and reliable.

Watt-Hour Meter - The watt-hour meter is shown in Figure 1. It consists of a Hall-effect multiplier, an operational amplifier, a capacitor, resistors, and a voltmeter. The Hall-effect multiplier produces an output proportional to the product of battery voltage and current.

The battery-voltage input to the Hall-effect multiplier has a resistor which limits input current to 250 milliamperes at a maximum battery voltage of 50 volts. The current input comes directly from a shunt.

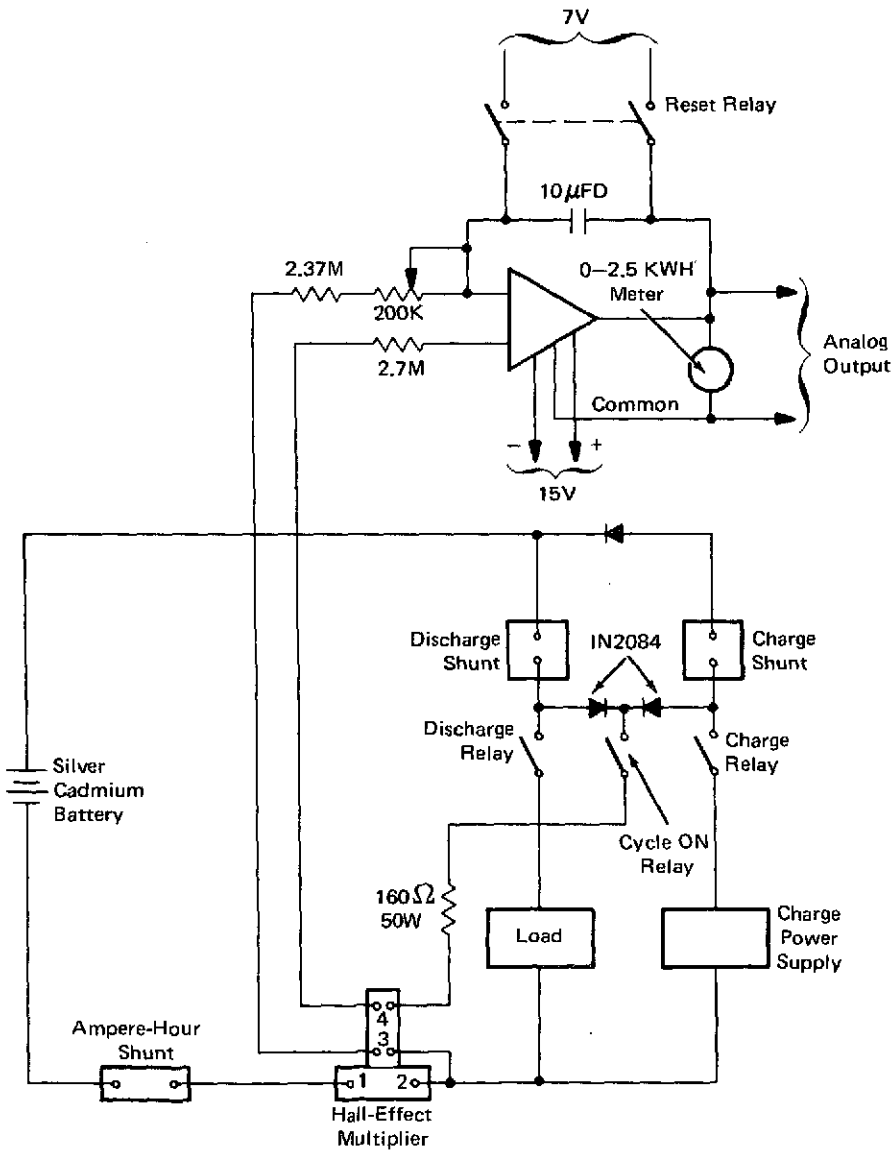


Figure 1. Watt-Hour Meter Schematic

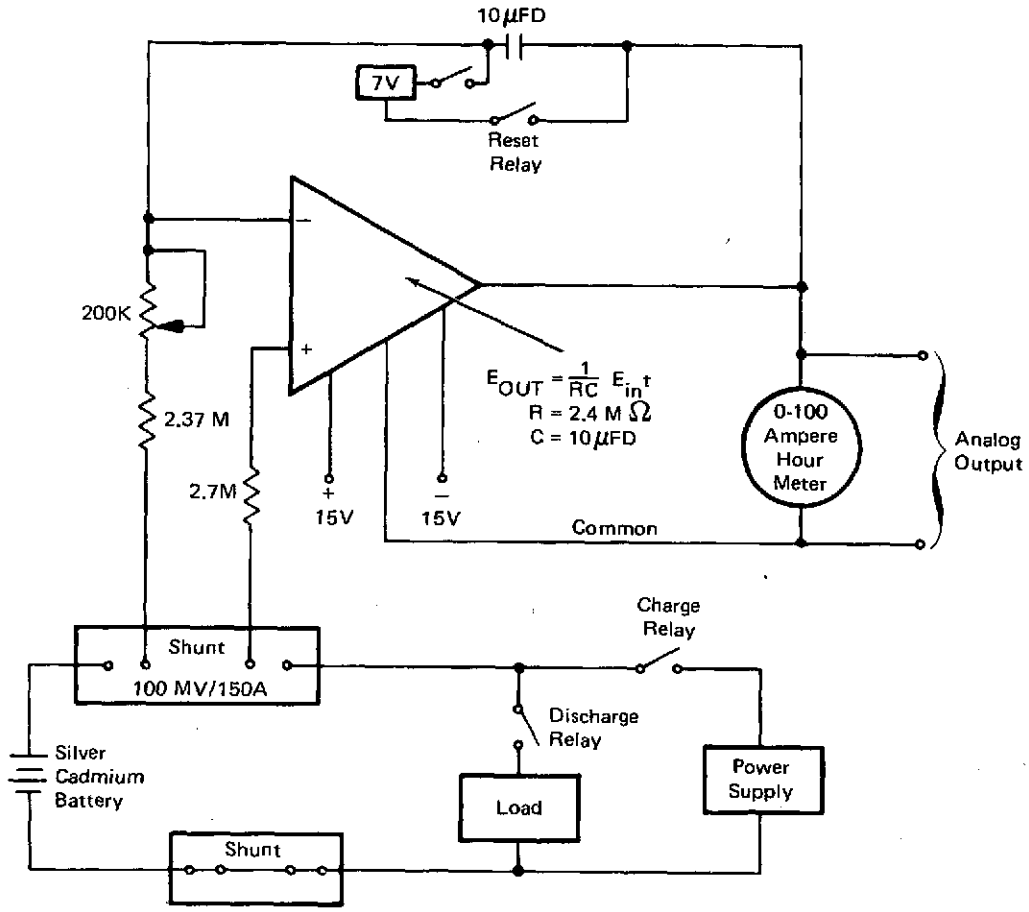


Figure 2. Ampere-Hour Schematic

The output of the Hall-effect multiplier is approximately 27 mV per watt. This voltage is fed to the operational amplifier where it is integrated to produce a signal proportional to watt-hours. The output of the operational amplifier is displayed on a voltmeter which is calibrated to read 250 watt-hours per volt. An analog output is also provided in addition to the meter display.

Ampere-Hour Meter - The ampere-hour meter has the same basic circuit as the watt-hour meter, but is modified as shown in Figure 2. It consists of an operational amplifier, a capacitor, resistors, a voltmeter, and a current shunt. To minimize error, the capacitor has a high insulation resistance, and the amplifier has low offset current and voltage. The input power for the operational amplifier is supplied by a +15, -15-volt regulated power supply. The amplifier output is 1 volt per 10 ampere-hours, with a range of 0 to 10 Vdc. An analog 0-to-10-volt signal is provided, in addition to the meter display.

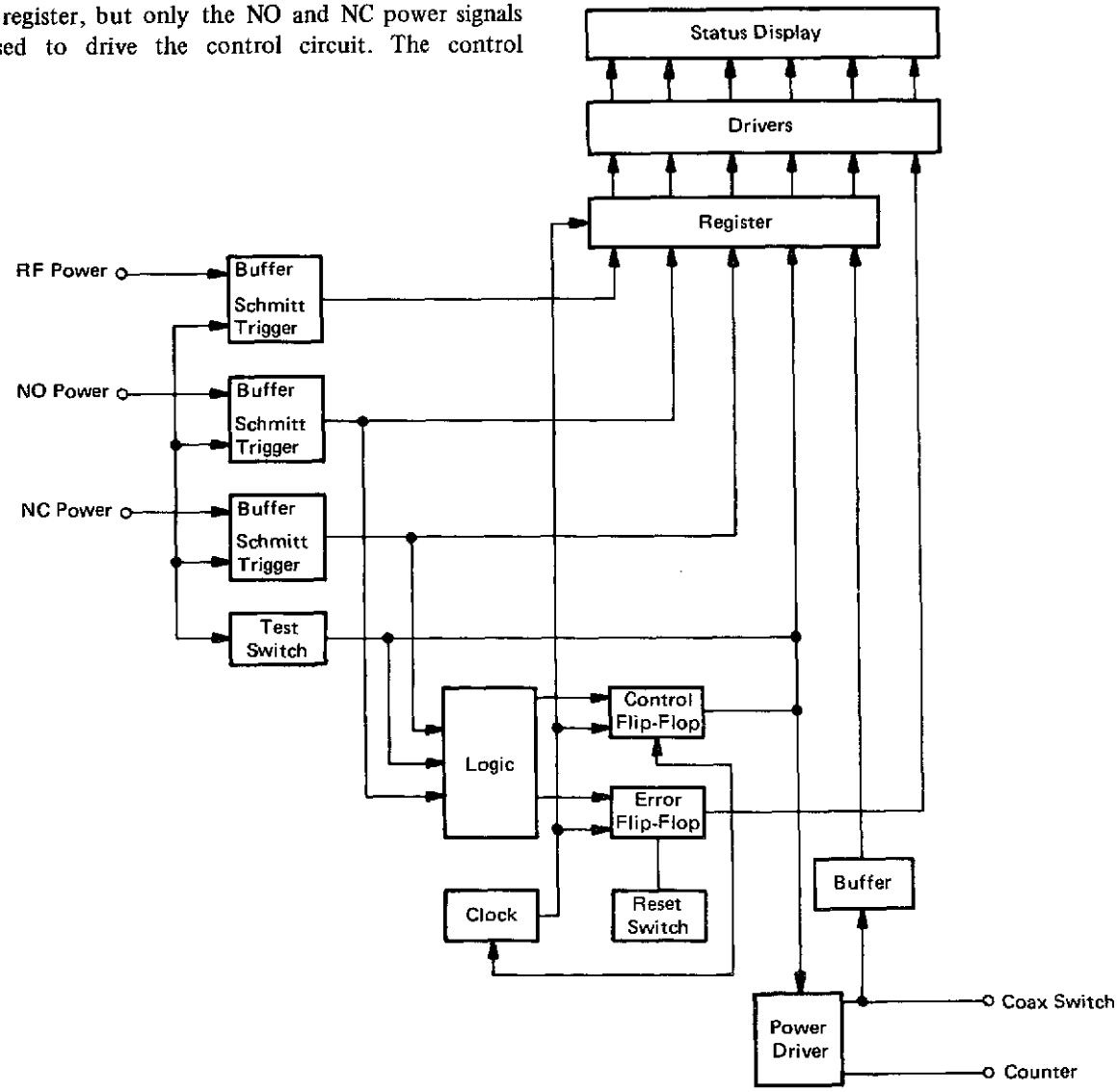
Source: A. D. Ciccanti and
R. J. Tallent of
Boeing Company
under contract to
Johnson Space Center
(MSC-11837)

No further documentation is available.

COAXIAL-SWITCH LIFE-TEST CONTROLLER

Logic circuitry is used to test automatically the life of coaxial switches. To detect failure, the test controller monitors RF input power, power out of the normally open (NO) port, and power out of the normally closed (NC) port.

The RF-detector negative-dc outputs are applied (see figure) to buffered Schmitt triggers where they are converted to normal logic signals. These signals are also simulated in the test-switch circuitry, for use in testing the controller and for driving a coaxial switch outside the RF test setup. All three signals are stored in the status register, but only the NO and NC power signals are used to drive the control circuit. The control circuit is three-state sequential composed of a control flip-flop, an error flip-flop, and associated components. Normally, the control flip-flop toggles on and off, driving the power drivers, the test simulator, and one bit of the status register. When an error is detected, the error flip-flop is set, which latches the control flip-flop off and disables the clock, locking the status register. The error flip-flop is displayed directly, without going through the status register. The last bit of the status register is driven from the output of the power driver



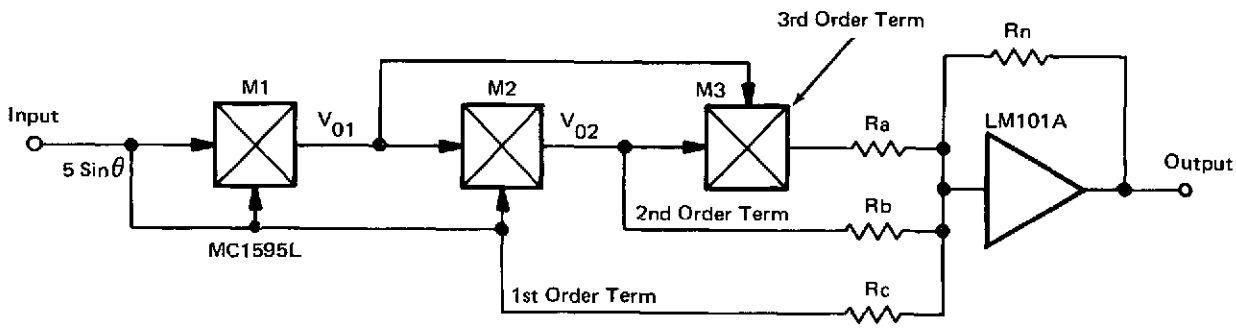
Coaxial-Switch Life-Test Controller

that drives the coaxial switch. The status register is updated on the leading edge of the positive clock pulse, and the control circuit is updated on the trailing edge. Thus, the status display always appears to be one step behind the coaxial switch; when an error occurs, the system status that existed when the error was detected is displayed.

Source: R. J. Lipin of
Sperry Rand Corp.
under contract to
Marshall Space Flight Center
(MFS-22336)

Circle 9 on Reader Service Card.

FOUR-QUADRANT MULTIPLIERS GENERATE SERIES EXPANSION OF SINUSOIDAL FUNCTIONS



Sinusoid Series-Expansion Circuit

Control-system functions frequently are only approximated due to difficulty in mechanizing multiplication functions. Often, an additional transducer must be used if two functions of the same variable are required. This method uses integrated-circuit multipliers to mechanize a three-term series expansion of a sinusoidal function. The demodulated sinusoidal output of a resolver is linearized to obtain angular information.

This angular information deviates from linearity by less than one-third of a degree at 45°. Accuracy can be improved by using a fourth term in the expansion instead of the three originally used.

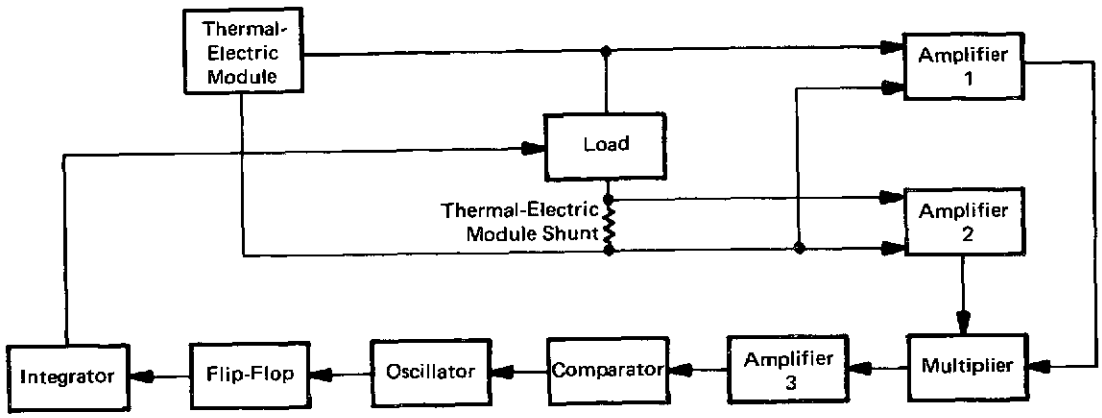
The first three terms of the expansion series for the sinusoidal function are first-, third-, and fifth-power terms of $\sin\theta$, each with a constant coefficient: $\theta = A\sin\theta + B\sin^3\theta + C\sin^5\theta$ ... . The circuit shown in the figure generates the terms in the following manner: The first-order input goes directly to a resistance (Rc) that fixes the coefficient. It is also fed to both inputs of the first multiplier (M1). The resulting second-order function and the first-order input are multiplied in M2. The output from this operation is sent directly to a coefficient resistor (Rb). In addition, this third-order signal and the second-order output of M2 are multiplied in M3. The resulting fifth-order signal picks up a coefficient from Ra. The composite linear output is normalized (Rn) and amplified.

An advantage of this series-expansion technique is that multiplication errors are divided by the series-expansion coefficient, and linearity is not disturbed near zero input.

Source: B. Bregman of
Martin Marietta Corp.
under contract to
Johnson Space Center
(MSC-13908)

No further documentation is available.

PEAK-POWER TRACKER CIRCUIT



Block Diagram of the Peak-Power Tracker Connected to the Thermal-Electric Module

DC power systems that transform heat energy into electrical energy must be prevented from overheating. Such overheating may result from either overloading or rapid unloading of the power source. Load fluctuations usually occur as various equipment items are turned on or off. To compensate for load fluctuations, parasitic loads or secondary power sources such as batteries are either added to or removed from the main bus. By maintaining a balanced load through the use of a peak-power tracker circuit, temperature degradation of a system is reduced, and the useful life of the primary power supply is increased. The peak-power tracker circuit combines a comparator, a gated oscillator, and a flip-flop with an integrator.

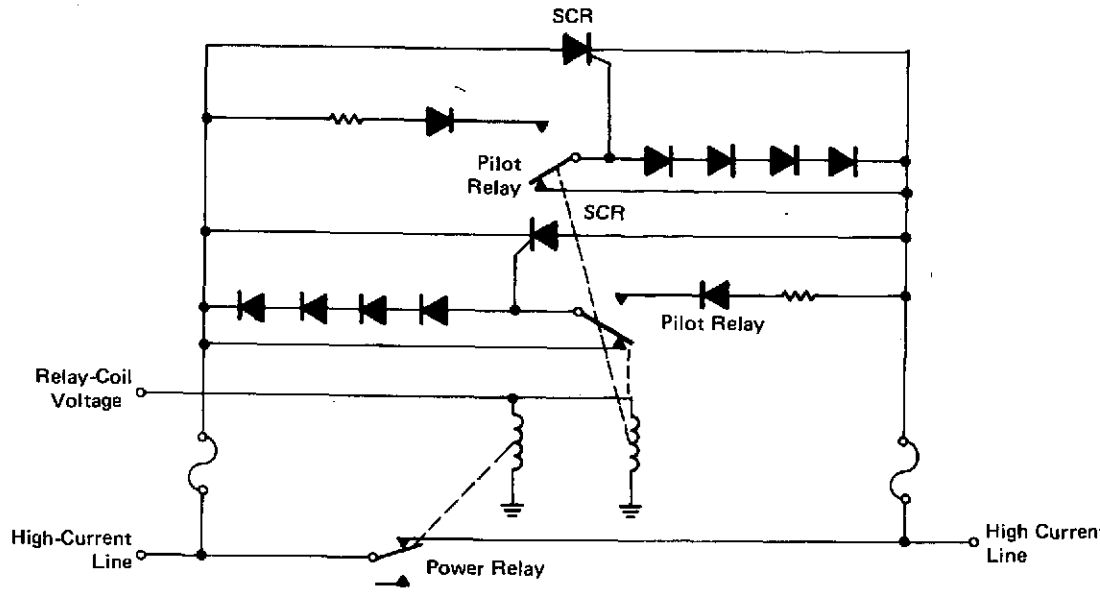
A prime future source of electrical energy is the thermal-electric module (TEM). The figure illustrates the use of the peak-power tracker with the TEM. Amplifiers 1 and 2 condition the current and voltage signals to levels suitable for the multiplier. Output of the multiplier is routed to amplifier 3 and fed into the comparator, which acts as a slope detector. The output of the comparator inhibits the oscillator when the slope of the power signal from the multiplier is positive. As the power goes through the peak point, the slope of the signal becomes negative, the comparator is switched off, and the oscillator is enabled.

The first pulse from the oscillator occurs, after a predetermined delay, and changes the state of the flip-flop. Output of the flip-flop signals the integrator to produce an output-voltage ramp, the slope of which is dependent on the state of the flip-flop. The integrator output is routed to the load, which uses current feedback to make the thermal-electric module-load current linearly dependent on the integrator-output voltage. The delay caused by the oscillator permits the load current to deviate from the peak-power point before the slope of the current perturbation is reversed. Slope reversal causes the power-signal slope to become positive, and the process is then repeated.

Source: R. V. Franklin of
Sperry Rand Corp.
under contract to
Marshall Space Flight Center
(MFS-22267)

Circle 10 on Reader Service Card.

SILICON-CONTROLLED RECTIFIER (SCR) PROTECTION OF RELAY CONTACTS



Relay-Contact Protection Circuit

High-current surges occasionally weld together relay contacts when filter capacitors charge or discharge at the instant of the relay closure. Any relay-contact "bounce" greatly increases the energy dissipation at the contact surface. Present solutions to the problem include the use of suppression capacitors across the relay contacts, inductors in series with the contacts, larger contact surfaces, or the use of special materials in the contacts themselves.

In the circuit shown, the current surge is bypassed around the relay contacts by shunting the high current through silicon-controlled rectifiers (SCR's), just prior to the instant of relay closure. The relay contacts close a few milliseconds later, and the steady-state current shuts off the SCR. Since the duty cycle of the SCR is essentially zero, no heat sinks are required. An auxiliary contact on the pilot relay shorts out the SCR gate-to-cathode circuit and makes the circuit immune to triggering by noise. Triggering with the anode voltage and with a clamped voltage from gate to cathode (using diodes) assures a sufficient triggering source at all voltage levels.

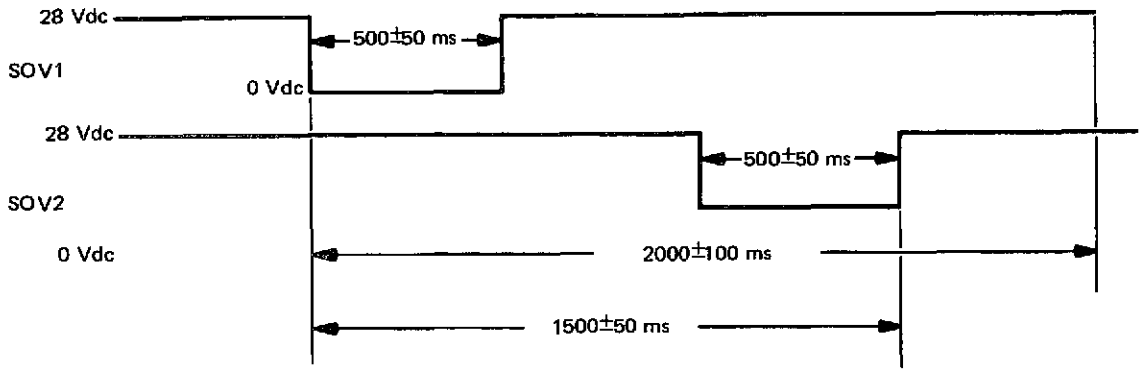
The pilot relay coil is energized simultaneously with the power relay coil. The operating time of the pilot relay is less than that of the larger power relay. When the pilot relay contacts close, the SCR is triggered by the positive anode voltage and conducts the transient current until the power relay contacts close a few milliseconds later.

This circuit may be used to connect power supplies containing large filter capacitors to supply lines or in other relay applications where current surge could damage relay contacts.

Source: D. L. Trower of
McDonnell Douglas Corp.
under contract to
Marshall Space Flight Center
(MFS-22444)

Circle 11 on Reader Service Card.

PNEUMATIC-IMPACT SOLENOID-VALVE DRIVER AND TIMER



Valve Driver-and-Timer Sequence (One Cycle)

A pneumatic-impact solenoid-valve driver and timer is used to test material samples, which are placed in a gaseous oxygen environment at pressures up to 69×10^6 N/m^2 (10,000 psi) and subjected to mechanical impact. As the materials are impacted, samples of possible combustion byproducts are taken 20 times at 2-second intervals.

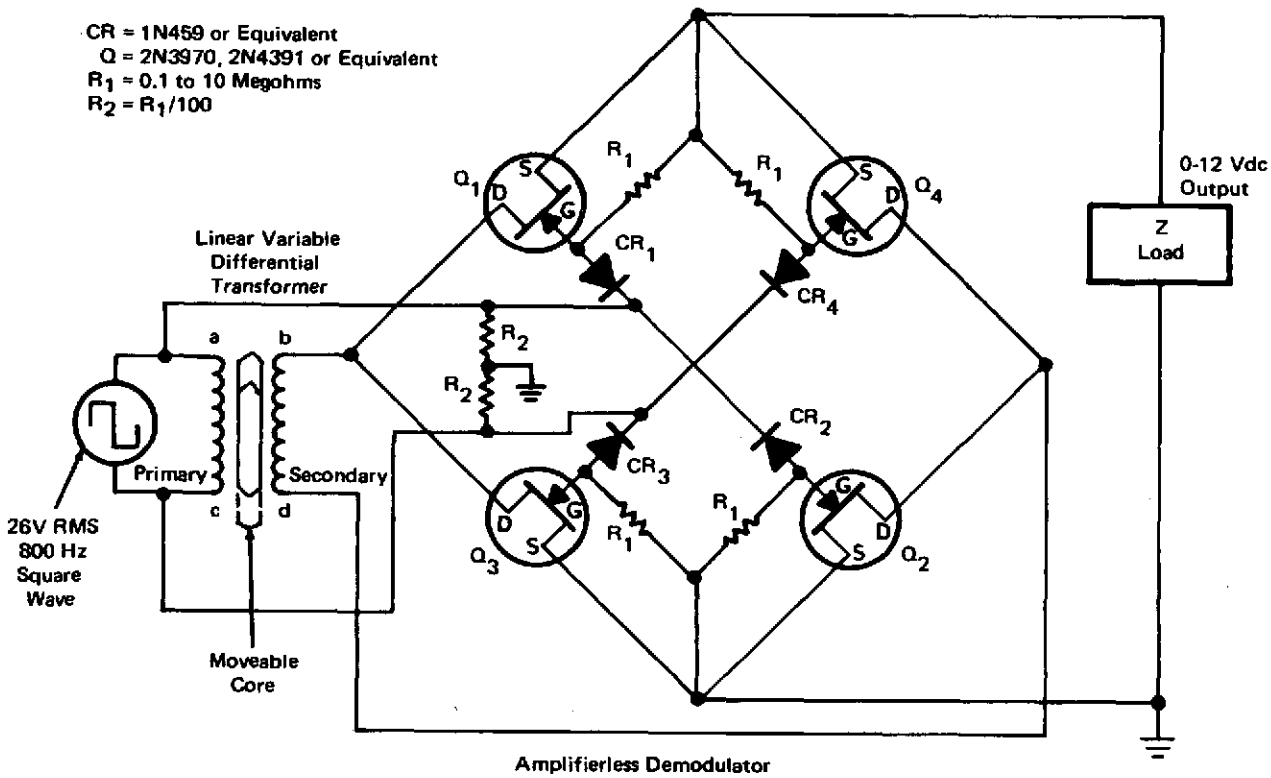
The driver and timer operate two valves, SOV1 and SOV2 (see figure), in the following sequence: Valve SOV1 closes to allow an enclosed impact of the sample; then it opens. Valve SOV2 then closes to allow sampling of the combustion byproducts; then it opens to complete one cycle.

The valve-driver circuit uses four cascaded stages of solid-state relaxation oscillators, having output pulse widths and frequencies that can be varied. The initial oscillator stage sets the 2-second time cycle, while the succeeding stages control pulse width and frequency. The output of the fourth (last) stage is fed to a counter circuit that is adjusted to conduct, when 20 complete cycles (40 output pulses) appear at the emitter of a unijunction transistor. This gates a silicon-controlled rectifier, which removes power from the driver-and-timer circuit. Logic circuitry generates the reset and start-of-sequence commands. The impact and sampling periods may be adjusted to accommodate a wide variety of materials for testing.

Source: D. L. Pippin of
Johnson Space Center and
L. A. Chavez of
Service Technology Corp.
under contract to
Johnson Space Center
(MSC-13623)

No further documentation is available.

AMPLIFIERLESS DEMODULATOR



Amplifierless Demodulator

This is a simple solid-state ac-to-dc demodulator that provides a ground-isolated, throttle-valve position signal to a computer from valve-drive amplifiers. It is accomplished without power from either the computer or the valve-drive amplifier dc supplies. The circuit uses four field-effect transistors (FET's) in a bridge configuration. They are switched on and off simultaneously, in opposite pairs, to provide full-wave rectification. The circuit is simple because the FET's can be biased more readily than conventional transistors. Prior art would require eight transistors and an eight-tap transformer.

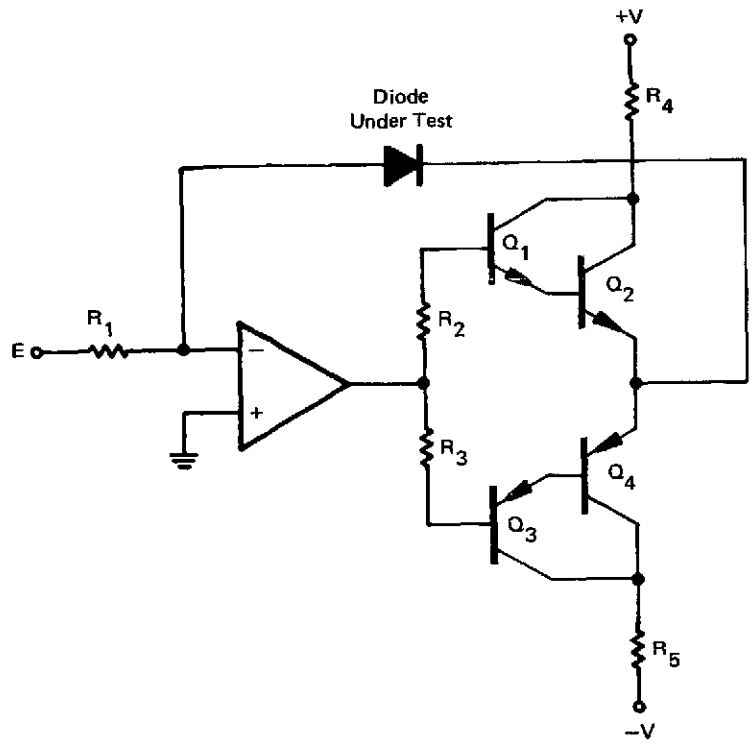
The throttle valve is linked to the movable core of the linear-variable differential transformer. Points a and c in the diagram alternate between +26 and –26 volts. The movable core regulates the voltage at b and d from 0 to +12 volts. When a is at +26 volts, b is at from 0 to +13 volts with respect to d (depending on the position of the core), e is +13, and f is –13 volts with respect to ground. Capacitors CR_1 and CR_2 are "off", and CR_3 and CR_4 are "on". A negative voltage appears on the gates of Q_3 and Q_4, turning them "off". Simultaneously, the gates of Q_1 and Q_2 are biased "on", permitting current flow from b through Q_1 to the load and through Q_2 to d. Conversely, when d becomes positive, Q_3 and Q_4 are "on", Q_1 and Q_2 are "off", and current flows from d through Q_4 to the load and through Q_3 to b.

This circuitry could be used in control systems that employ ac-position or rate-sensor pickoffs. It could also be used in ac-to-dc systems with large primary voltages and smaller secondary voltages (sufficient to control FET's).

Source: Melvin M. Hintze of
Martin Marietta Corp.
under contract to
Langley Research Center
(LAR-10758)

No further documentation is available.

OPERATIONAL AMPLIFIER ELIMINATES DIODE FORWARD-VOLTAGE DROP



Forward-Voltage-Drop Compensating Circuit

In a radiation-effects test program, measurement of the forward-voltage drop of silicon-controlled rectifiers (SCR's) became a problem in equipment design. Circuit considerations required that all voltage requirements be made with respect to a ground reference established at the cathode of the SCR. This necessarily would include the forward-voltage drop of the SCR, which was known to increase significantly in the presence of radiation. Valid measurement of current through the SCR required elimination of the forward-voltage-drop effect.

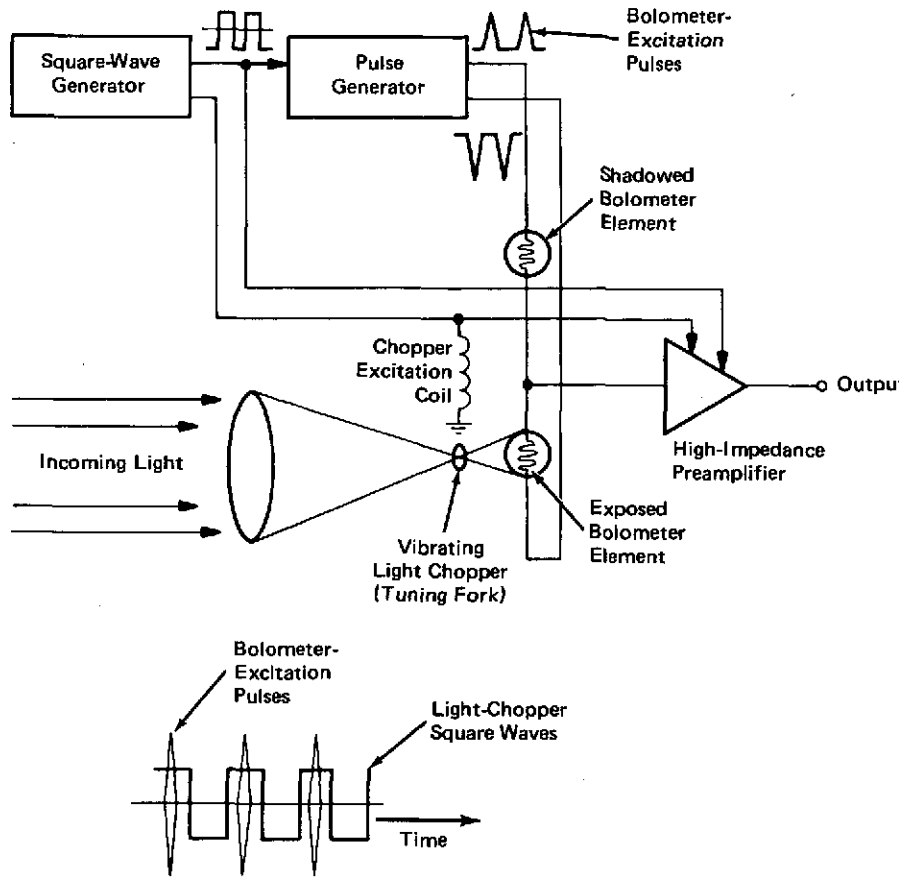
The problem was solved by inserting the SCR into the feedback loop (see figure) of an operational amplifier, in series with a transistorized power stage. For simplicity, the SCR is shown as a diode in the figure. Because the amplifier gain is proportional to the feedback impedance, a change in the forward-voltage drop reflects a similar change in amplifier gain and hence output. Voltage output of the amplifier equals the SCR forward-voltage drop and is of opposite polarity to that of the input. Thus, the forward-voltage drop is effectively cancelled by the amplifier.

Because the summing point of the operational amplifier is essentially at ground potential, current through the SCR can be deduced by knowing the values of input voltage E and of resistor R_1, and therefore determining input current, approximately equal to feedback current.

Source: Edward A. Maslowski
Lewis Research Center
(LEW-10716)

No further documentation is available.

PULSE-EXCITED BOLOMETER



Pulse-Excited Bolometer System

In order to increase the signal-to-noise ratio of a bolometer sensor, a conventional square-wave generator and a light chopper are used to furnish excitation pulses to the bolometer bridge.

The square-wave generator (see figure) drives the light chopper to impose a square-wave train of light pulses on the exposed bolometer element. These excitation pulses are applied to the two-element bolometer bridge, during a very short interval in the center of each light pulse falling on the exposed bolometer element. The preamplifier output signal is a product of the incident radiation on the exposed bolometer element and the bridge excitation, and it is proportional to the excitation amplitude.

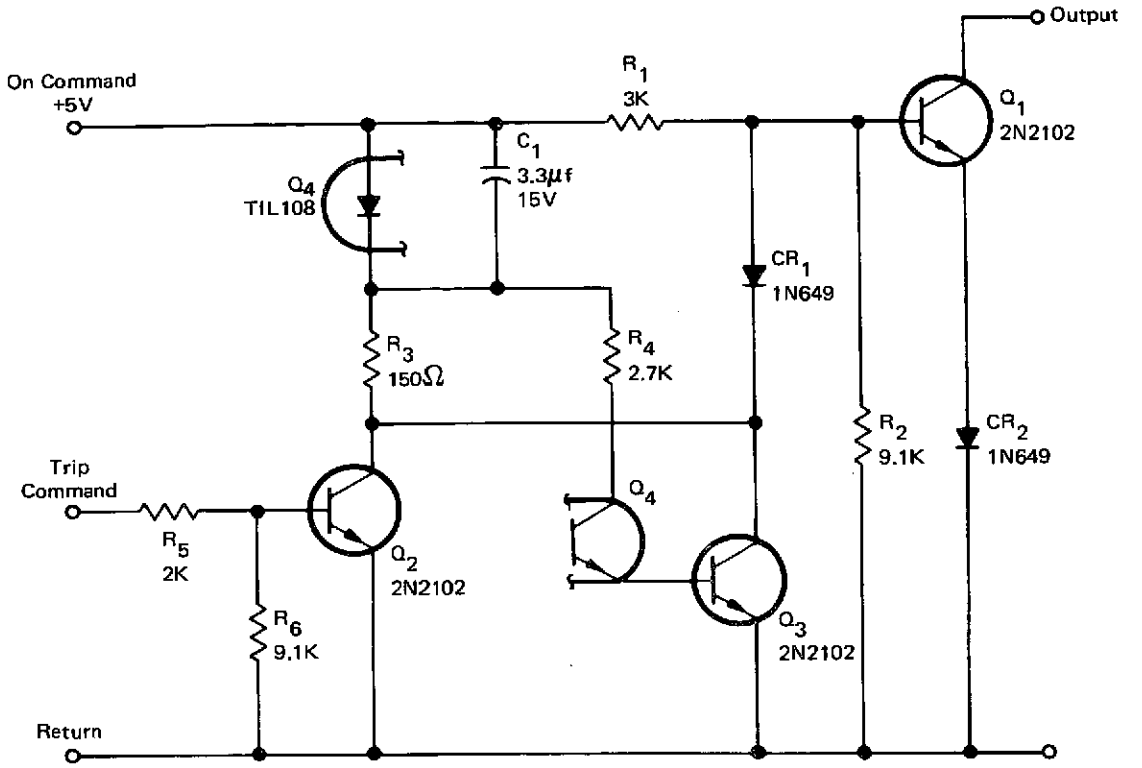
Bolometer heating is proportional to both excitation amplitude and duty cycle. Since the pulse excitation reduces the bolometer-current duty cycle, the heating is significantly reduced. High-amplitude signals are generated without undue heating of the bolometer sensor.

This pulse-excitation technique could be used to increase bolometer sensitivity, by permitting a higher applied voltage to a given bolometer than is possible by conventional ac or dc excitation.

Source: Stanley J. Rusk of
Lockheed Missiles and Space Co.
under contract to
Ames Research Center
(ARC-10292)

No further documentation is available.

5-VOLT COMMAND TRIP-AND-HOLD CIRCUIT



Trip-and-Hold Circuit

A switching circuit has been developed to control high-voltage devices from 5-volt command signals. This solid-state circuit has a much faster response time than electromechanical relays. The command signal can be initiated by one or more sensor inputs that respond to conditions such as temperature or pressure.

The circuit is shown in the figure. A trip command causes a transistor (Q_2 in the figure) to conduct; this actuates the optical isolator (Q_4) which, in turn, causes Q_3 to conduct.

Feedback from the collector of Q_3 to the collector of Q_2 maintains a current flow through Q_4, even if the trip-command signal is removed. The circuit remains in this latched state until the 5-volt "on" command is removed. The output state (Q_1) is a current sink to ground configuration.

Source: C. E. Whaley of
Sperry Rand Corp.
under contract to
Marshall Space Flight Center
(MFS-22682)

Circle 12 on Reader Service Card.

ELECTROMECHANICAL EVENT-SEQUENCING SYSTEM

An electromechanical event-sequencing system has been developed for photographic cameras. The system consists of four subsystems: (1) a power supply, (2) a control unit, (3) a light source, and (4) a motor and solenoid.

The power supply is a rechargeable nickel/cadmium cell, consisting of four commercially available batteries in a 12.5-volt series-parallel arrangement. The control unit contains two parts: (1) a monostable relay driver that generates a 100-millisecond solenoid pulse and (2) logic that programs a film-advance motor.

The light source is a linear flashtube with a modified reflector, and it has an energy level of 8.1 watt-seconds. Circuitry with the light flasher consists primarily of a dc/dc converter, a voltage sensor, an energy-storage element, and a flashtube-trigger circuit.

The system requires a 12-volt motor, though it has been used with a 28-volt motor that meets the speed-torque requirements at 12 volts. Selection of the solenoid is based on the force required to displace a shutter star wheel in the camera: 14.6 watts for the camera in this system.

All the components are housed in a compact unit and require little maintenance, even under rather extreme conditions.

Source: Eastman Kodak Company
under contract to
Johnson Space Center
(MSC-13620)

Circle 13 on Reader Service Card.

Patent Information

The following innovations, described in this Compilation, have been patented or are being considered for patent action as indicated below:

Permalloy Patchwork Improves Bubble-Domain Memory Device (Page 1) MFS-22116

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the IBM Corp., Huntsville, Alabama 35805.

Bias-Field Equalizer for Bubble-Domain Memories (Page 3) MFS-21913

Thermal Control of Operating Margins in Bubble-Domain Memory Devices (Page 3) MFS-22115

Edge Effect Improves Bubble-Domain Memory Devices (Page 4) MFS-22114

Coaxial-Switch Life-Test Controller (Page 18) MFS-22336

Peak-Power Tracker Circuit (Page 20) MFS-22267

Silicon-Controlled Rectifier (SCR) Protection of Relay Contacts (Page 21) MFS-22444

5-Volt Command Trip-and-Hold Circuit (Page 26) MFS-22682

Inquiries concerning rights for the commercial use of these inventions should be addressed to:

Patent Counsel
Marshall Space Flight Center
Code A&PS-PAT
Marshall Space Flight Center, Alabama 35812

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